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09/846,085	04/30/2001	Michael T. Zhang	INTL-0578-US (P11466)	3980

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EXAMINER
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CHANDRASEKHAR, PRANAV

ART UNIT	PAPER NUMBER
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2115

DATE MAILED: 03/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

09/846,085

**Applicant(s)**

ZHANG, MICHAEL T.

**Examiner**

Pranav Chandrasekhar

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 April 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-27 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |                                                                                                                        |                                                                                         |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                            | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____                                                |

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Regarding claims 11,18,19,21,24 and 26, the word 'near' with reference to level of supply voltage does not clearly indicate the proximity of the value of supply voltage level to the desired voltage level.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Voegeli et al [US Pat No. 6,448,672] in view of Isaac et al [US Pat No. 6,327,663].

3. As per claim 1, Voegeli teaches

an external supply voltage terminal [6 Fig 1; col. 4 lines 50-53];

a circuit to provide an indication of a first supply voltage level to be furnished to the supply voltage terminal in response to receiving power from the backplane [col. 11 lines 47-53; col. 2 lines 25-29; col. 10 lines 29-33; col. 10 lines 46-50. The indication being provided to the power supply by the parameter register is viewed as a response to the circuit receiving power from the backplane].

Voegeli does not explicitly teach a circuit providing an indication of a first supply voltage level to the same supply voltage terminal that it receives power from.

Isaac teaches a system in which the circuit is powered by the voltage supply terminal to which it indicates a voltage level [710 Fig. 5; col. 7 lines 13-37. Fig 5 suggests that the circuit 710 does not receive power from any other source besides power supply 30 (supply voltage terminal).].

It would have been obvious to one skilled in the art to combine the teachings of Voegeli and Isaac to use a single supply voltage terminal to power the circuit that provides the indication of supply voltage level and to receive the supply voltage level to be furnished in order to avoid using two separate supply voltage terminals.

4. As per claim 11, Voegeli teaches

providing an indication of a first supply voltage level to be furnished to a supply voltage terminal in response to receiving power from the backplane [Fig 7; col. 11 lines 47-53; col. 2 lines 25-29; col. 10 lines 29-33; col. 10 lines 46-50. The indication being provided by the parameter register to the power supply is viewed as a response to the circuit receiving power from the backplane.]; and

in response to the indication, establishing a voltage of the terminal near the first supply voltage level [col. 13 lines 15-20; col. 13 lines 43-48].

Voegeli does not explicitly teach a circuit providing an indication of a first supply voltage level to the same supply voltage terminal that it receives power from.

Isaac teaches a system in which the circuit is powered by the voltage supply terminal to which it indicates a voltage level [710 Fig. 5; col. 7 lines 13-37. Fig 5

suggests that the circuit 710 does not receive power from any other source besides power supply 30 (supply voltage terminal).].

5. As per claim 18, Voegeli teaches

an electronic device including an external supply voltage terminal [6 Fig 1; col. 4 lines 50-53], the electronic device providing an indication of a first supply voltage level to be furnished to the terminal in response to receiving power from the backplane [Fig 7; col. 11 lines 47-53; col. 2 lines 25-29; col. 10 lines 29-33; col. 10 lines 46-50. The indication being provided to the power supply is viewed as a response to the circuit receiving power from the backplane.]; and

a backplane to provide power to the electronic device to cause the electronic device to provide the indication [col. 11 lines 47-53];

a voltage regulator to regulate a voltage of the terminal near the first supply voltage level in response to the electronic device providing the indication [col. 13 lines 15-20; col. 4 lines 50-53; col. 11 lines 47-53; col. 13 lines 43-48].

Voegeli does not teach the electronic device providing an indication of a first supply voltage level to the same supply voltage terminal that it receives power from. Furthermore, Voegeli does not teach a voltage regulator providing power to the electronic device causing it to provide the indication.

Isaac teaches a system in which the electronic device is powered by the voltage supply terminal to which it indicates a supply voltage level [710 Fig 5; col. 7 lines 13-37. Fig 5 suggests that the circuit 710 does not receive power from any other source besides power supply (supply voltage terminal).]. Furthermore, Isaac teaches a

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voltage regulator providing power to the electronic device causing it to provide the indication [30 Fig 5; 40 Fig 2. The power supply 30 of Fig 5 is shown to contain a voltage regulator in Fig 4. Hence, the electronic device is viewed as receiving power from the voltage regulator to provide the indication].

It would have been obvious to one skilled in the art to combine the teachings of Voegeli and Isaac to use a single power supply (with a voltage terminal and voltage regulator) to power the circuit that provides the indication of supply voltage level and to receive the supply voltage level to be furnished in order to avoid the need to use two different supply voltage terminals.

6. As per claim 24, Voegeli teaches

voltage regulation circuitry to provide an output voltage in response to a reference voltage to power an electronic device [col. 4 lines 47-53; col. 2 lines 25-29; col. 11 lines 47-53; col. 13 lines 15-20; col. 13 lines 43-48]

a circuit to set the reference voltage to a first level to cause its output to be at a predetermined output voltage level [col. 11 lines 47-48; col. 4 lines 15-17], and in response to an indication of a supply voltage level furnished by the electronic device, to cause the voltage regulation circuitry to regulate its output voltage near the supply voltage level indicated by the electronic device [col. 11 lines 47-53; col. 4 lines 47-53; col. 13 lines 15-20; col. 2 lines 25-30; col. 8 lines 31-35; col. 13 lines 43-48].

Voegeli does not explicitly teach a single voltage regulation circuitry regulating the output voltage near a predetermined output voltage level and changing this level to that of a second supply voltage level as indicated by the electronic device.

Isaac teaches a single voltage regulator regulating the output for the voltage indicating unit and then to a second supply voltage level as indicated by the electronic device [30 Fig 5; 40 Fig 2; col. 7 lines 13-37. The power supply 30 of Fig 5 is shown to contain a voltage regulator in Fig 4. Hence, the electronic device is viewed as receiving a regulated output voltage from the voltage regulator. This voltage is viewed as having a default value (predetermined output value). Furthermore, the same voltage regulator regulates its output to a second supply voltage level as indicated by the voltage indicating device 710 of Fig. 5].

7. As per claims 2 and 12, Voegeli further teaches the circuit providing the indication in response to a second supply voltage level being furnished by the backplane, the second supply voltage level being independent from the indication [col. 11 lines 47-53; col. 4 lines 15-17].

Voegeli does not explicitly teach a circuit providing an indication of a first supply voltage level to the same supply voltage terminal in response to a second supply voltage level furnished to the terminal.

Isaac teaches a system in which the circuit is powered by the voltage supply terminal with a second supply voltage level in response to which it indicates a first supply voltage level [710 Fig. 5; col. 7 lines 13-37. Fig 5 suggests that the circuit 710 does not receive power from any other source besides power supply 30 (supply voltage terminal).].

8. As per claims 3, 13, 20 and 25, Voegeli further teaches the second supply voltage level to comprise a relatively constant supply voltage level [col. 4 lines 15-17].

9. As per claims 4 and 14, Voegeli further teaches another circuit separate from the first circuit to receive the first voltage supply level from the terminal [col. 11 lines 50-53; col. 13 lines 15-20; col. 12 lines 12-14].

10. As per claim 5, Voegeli does not explicitly teach the said another circuit to comprise the core circuitry of a central processing unit device.

Isaac teaches the said another circuit to be a processor [10 Fig 2; col. 5 lines 56-67];

It would have been obvious to modify the teachings of Voegeli and Isaac to circuit to comprise the core circuitry of a central processing unit device.

11. As per claim 6, Voegeli and Isaac do not explicitly teach a die wherein said another circuit and the first circuit are fabricated on the die.

It would have been obvious to modify the teachings of Voegeli and Isaac to fabricate the first circuit and the said another circuit on a die.

12. As per claims 7 and 15, Voegeli further teaches the circuit furnishing the indication in response to a second supply voltage level being furnished by the backplane [col. 11 lines 46-48; col. 4 lines 15-17].

Isaac teaches the circuit [710 Fig 5] furnishing the indication in response to a second supply voltage level being furnished by the supply terminal [30 Fig 5].

Voegeli and Isaac do not explicitly teach furnishing a first voltage supply level to the terminal in response to validation of the indication.

It would have been obvious to one skilled in the art to modify the teachings of Isaac and Voegeli to ensure that the indication is valid prior to furnishing the first voltage

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supply level to the terminal to avoid causing damage to any of the devices powered by the supply terminal due to furnishing of an incorrect value of supply voltage.

13. As per claims 8,16 and 22, Voegeli does not explicitly teach the electronic device comprising a central processing unit device.

Isaac teaches the electronic device comprising a processor [10 Fig 1];

It would have been obvious to one skilled in the art to modify the teachings of Voegeli and Isaac to incorporate a central processing unit device in the electronic device.

14. As per claims 9,17 and 23, Voegeli further teaches the indication representing a voltage identification number [col. 11 lines 47-53; col.6 lines 18-20; Table 2].

15. As per claim 10, Voegeli does not explicitly teach the circuit not receiving power other than through the terminal.

Isaac teaches the circuit not receiving power other than through the terminal [710 Fig 5. Fig 5 suggests that the circuit 710 receives power only from power supply 30].

16. As per claim 19, Voegeli further teaches the voltage regulator providing the indication in response to a second supply voltage level being furnished by the backplane, the second supply voltage level being independent from the indication [col. 11 lines 47-53; col. 4 lines 50-53].

Voegeli does not explicitly teach a voltage regulator providing an indication of a first supply voltage level to the same supply voltage terminal in response to a second supply voltage level furnished to the terminal.

Isaac teaches a system in which the circuit is powered by the voltage regulator with a second supply voltage level in response to which it indicates a first supply voltage level [710 Fig. 5; col. 7 lines 13-37. Fig 5 suggests that the circuit 710 does not receive power from any other source besides power supply 30 (supply voltage terminal). The power supply 30 of Fig 5 contains a voltage regulator as shown in Fig 4. Hence, it is viewed the electronic device provides the indication in response to a second supply voltage level from the voltage regulator 40 of Fig 4].

It would have been obvious to one skilled in the art to combine the teachings of Voegeli and Isaac to use a single supply voltage regulator (with a supply terminal) to furnish a second supply voltage level that causes the indication of a first supply voltage level that is independent of the second supply voltage level to avoid the need to use two different supply voltage terminals.

17. As per claim 21, Voegeli further teaches the electronic device furnishing the indication in response to a second supply voltage level being furnished by the backplane [col. 11 lines 46-48; col. 4 lines 15-17].

Isaac teaches the electronic device [710 Fig 5] furnishing the indication in response to a second supply voltage level being furnished by the supply terminal of the voltage regulator [30 Fig 5. The power supply 30 of Fig 5 is shown to have a voltage

regulator in Fig 4. Hence the voltage regulator is viewed as furnishing a second supply voltage level to the circuit].

Voegeli and Isaac do not explicitly teach furnishing a first voltage supply level to the terminal in response to validation of the indication.

It would have been obvious to one skilled in the art to modify the teachings of Isaac and Voegeli to ensure that the indication is valid prior to furnishing the first voltage supply level to the terminal to avoid causing damage to any of the devices powered by the voltage regulator due to furnishing of an incorrect value of supply voltage.

18. As per claim 26, Voegeli further teaches the electronic device furnishing the indication in response to an output voltage at a predetermined output voltage level [col. 11 lines 47-53; col. 4 lines 15-17].

Voegeli does not explicitly teach the output voltage being regulated.

Isaac teaches the output voltage being regulated [Fig 5; Fig 4. The power supply 30 of Fig 5 is shown to have a voltage regulator in Fig 4. With regard to figure 5, it is evident that the electronic device 710 does not receive power from any source besides the power supply. Prior to the power supply powering on the processor, a default voltage level having a predetermined value must be regulated to the electronic device 710]

19. As per claim 27, Voegeli further teaches the indication representing a voltage identification number [col. 11 lines 47-53; col.6 lines 18-20; Table 2].

Voegeli does not explicitly teach the electronic device comprising a central processing unit.

Isaac teaches the electronic device comprising a processor [10 Fig 1];

It would have been obvious to one skilled in the art to modify the teachings of Voegeli and Isaac to incorporate a central processing unit device in the electronic device.

### ***Conclusion***

20. An examination of this application reveals that applicant is unfamiliar with patent prosecution procedure. While an inventor may prosecute the application, lack of skill in this field usually acts as a liability in affording the maximum protection for the invention disclosed. Applicant is advised to secure the services of a registered patent attorney or agent to prosecute the application, since the value of a patent is largely dependent upon skilled preparation and prosecution. The Office cannot aid in selecting an attorney or agent.

Applicant is advised of the availability of the publication "Attorneys and Agents Registered to Practice Before the U.S. Patent and Trademark Office." This publication is for sale by the Superintendent of Documents, U.S. Government Printing Office, Washington, D.C. 20402.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pranav Chandrasekhar whose telephone number is 703-305-8647. The examiner can normally be reached on 8:30 a.m.-5:00 p.m..


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 703-305-9717. The fax phone

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numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Pranav Chandrasekhar  
March 23, 2004



THOMAS LEE  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100